



Phase Locked Loop Design as a Frequency Multiplier

By George Tom Varghese

LAP Lambert Academic Publishing Okt 2012, 2012. Taschenbuch. Book Condition: Neu. 220x150x5 mm. This item is printed on demand - Print on Demand Neuware - High-performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Phase locked-loops (PLLs) are widely used to generate well-timed on-chip clocks in high-performance digital systems. A PLL is a closed loop frequency system that locks the phase of an output signal to an input reference signal. PLL s are widely used in computer, radio, and telecommunications systems where it is necessary to stabilize a generated signal or to detect signals. The term lock refers to a constant or zero phase difference between two signals. The signal from the feedback path is compared to the input reference signal, until the two signals are locked. If the phase is unmatched, this is called the unlocked state, and the signal is sent to each component in the loop to correct the phase difference. These components consist of the Phase Frequency Detector (PFD), the charge pump (CP), the low pass filter (LPF), the voltage controlled oscillator (VCO)...



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